

FIG. 2 (Amended)

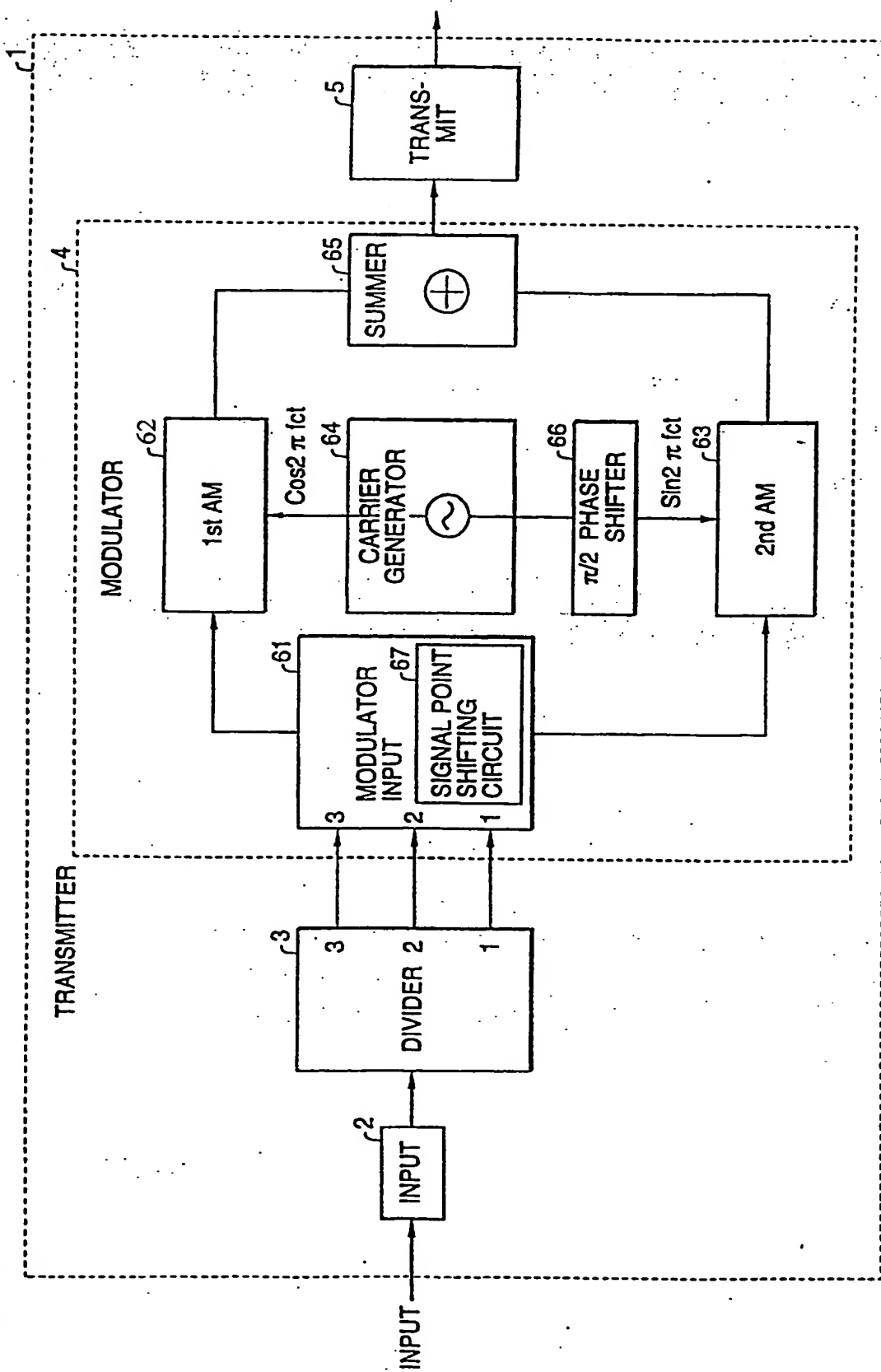


FIG. 10 (Amended)

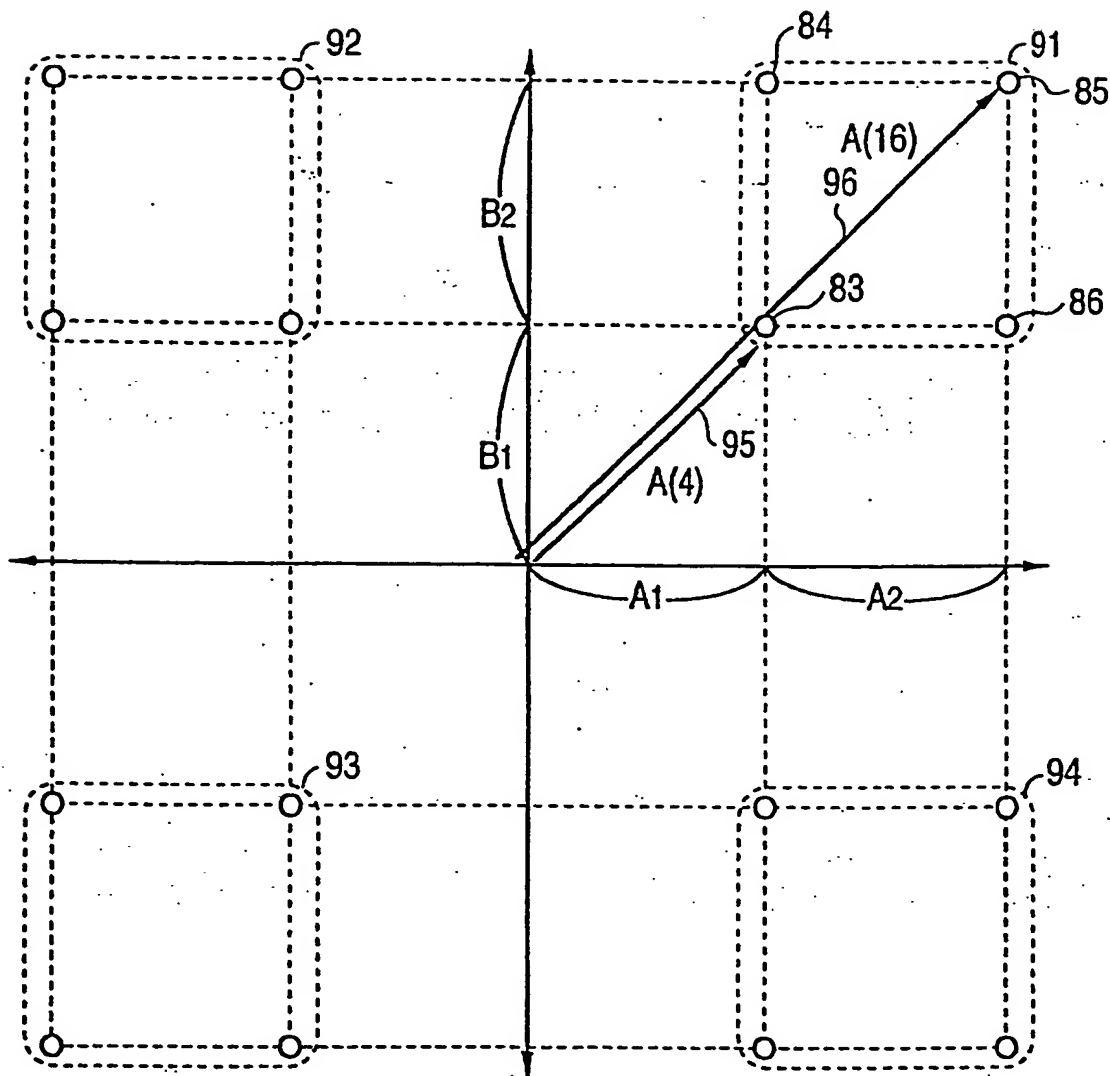


FIG. 17 (Amended)

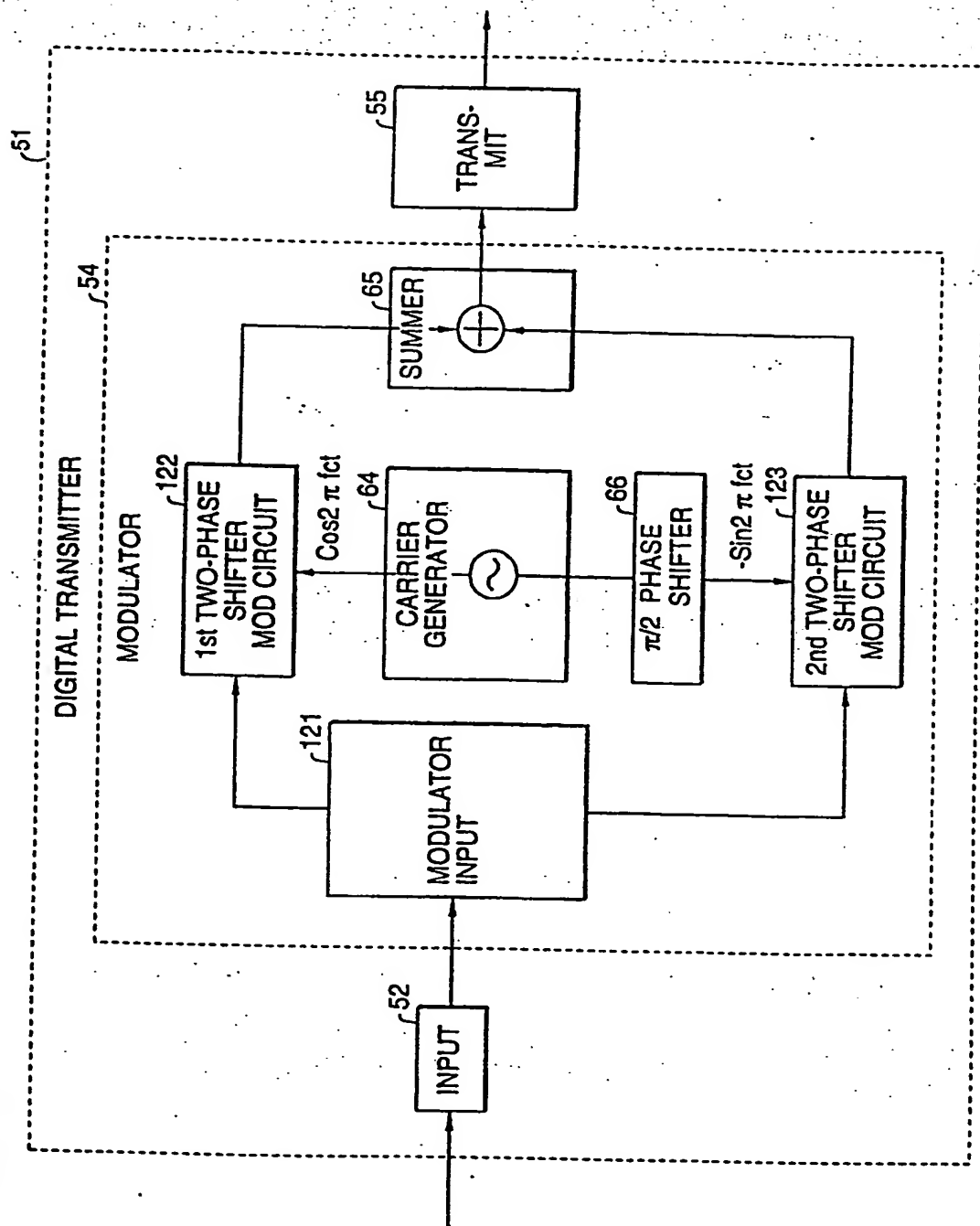


FIG. 29 (Amended)

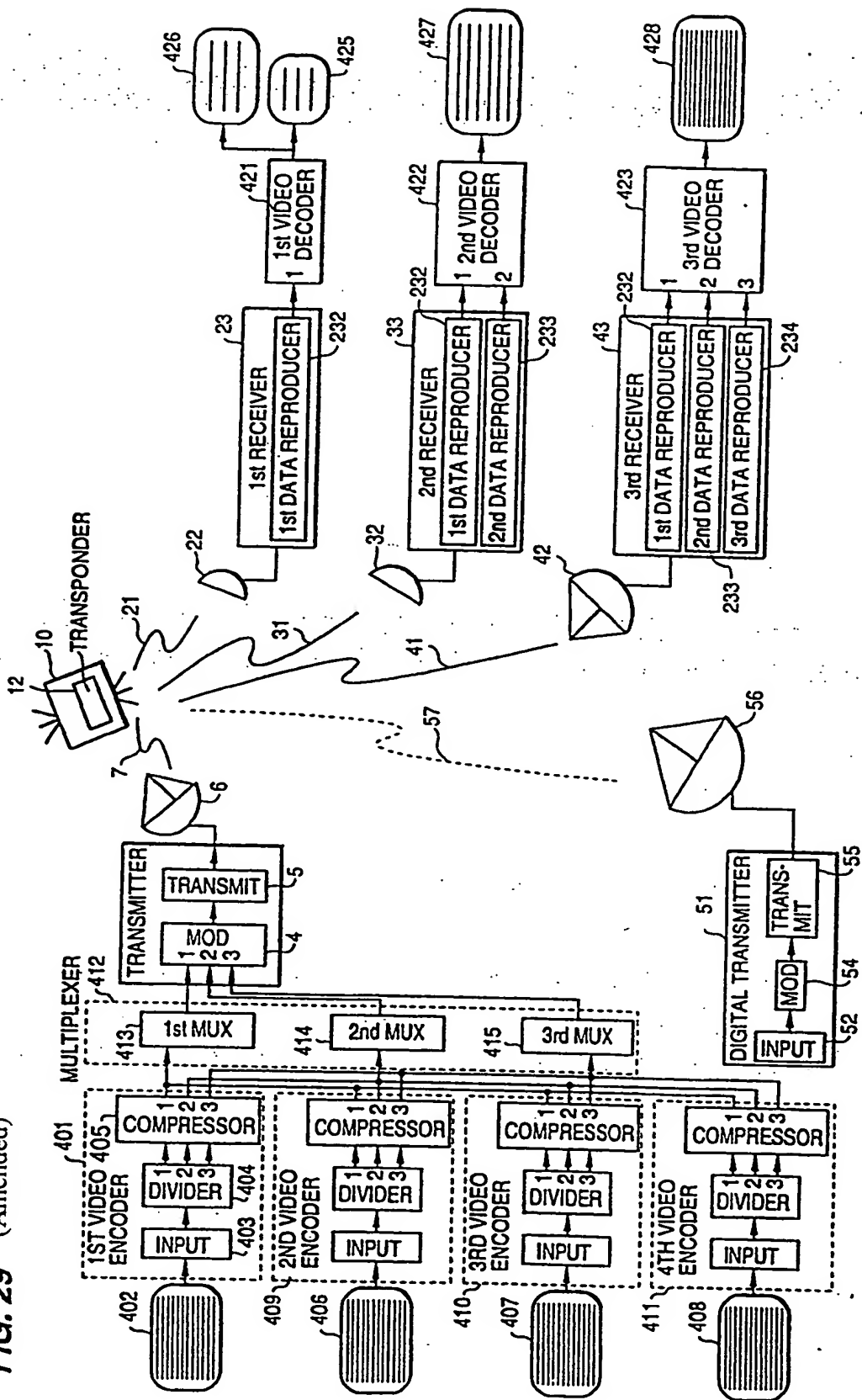


FIG. 48.

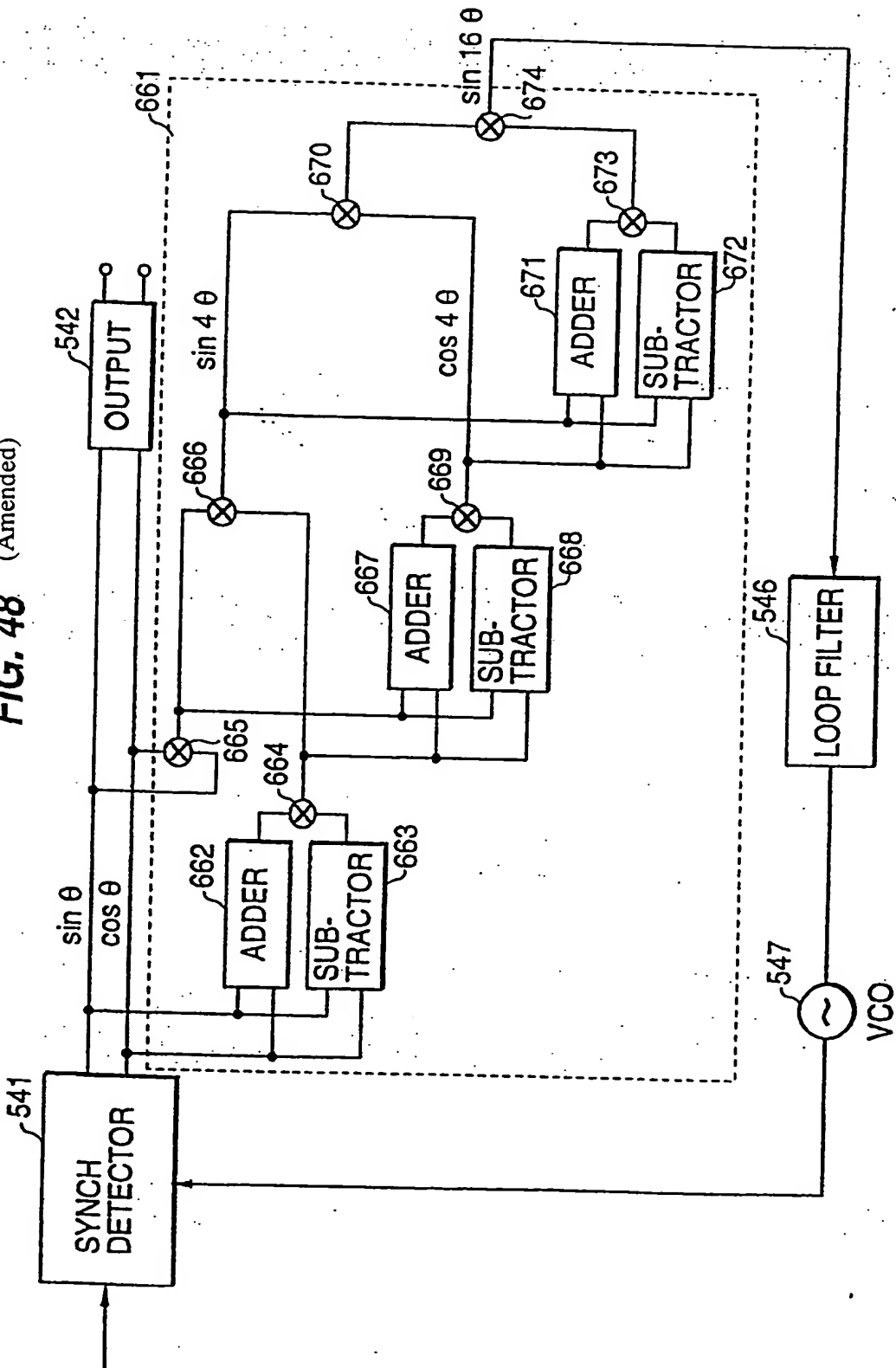
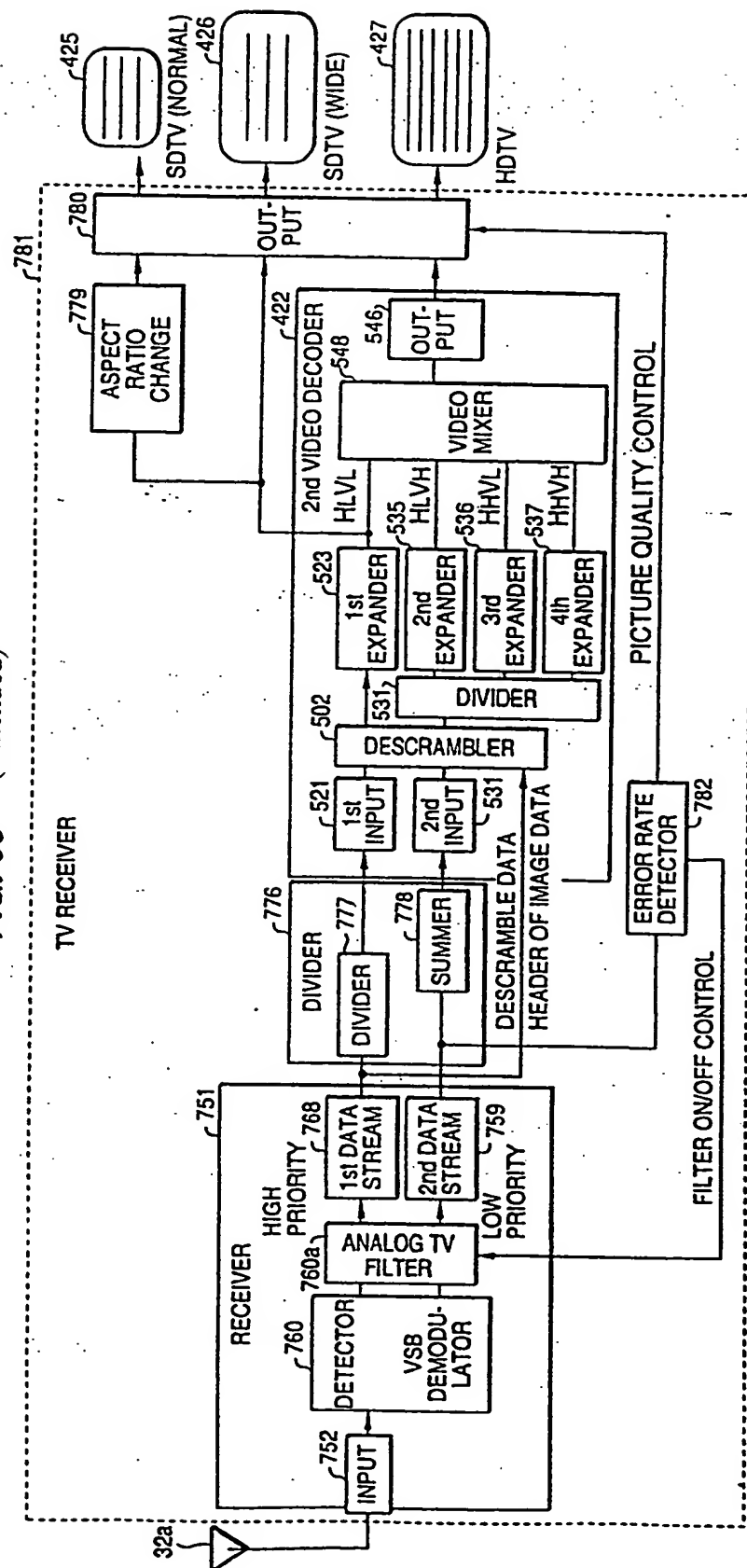


FIG. 65 (Amended)



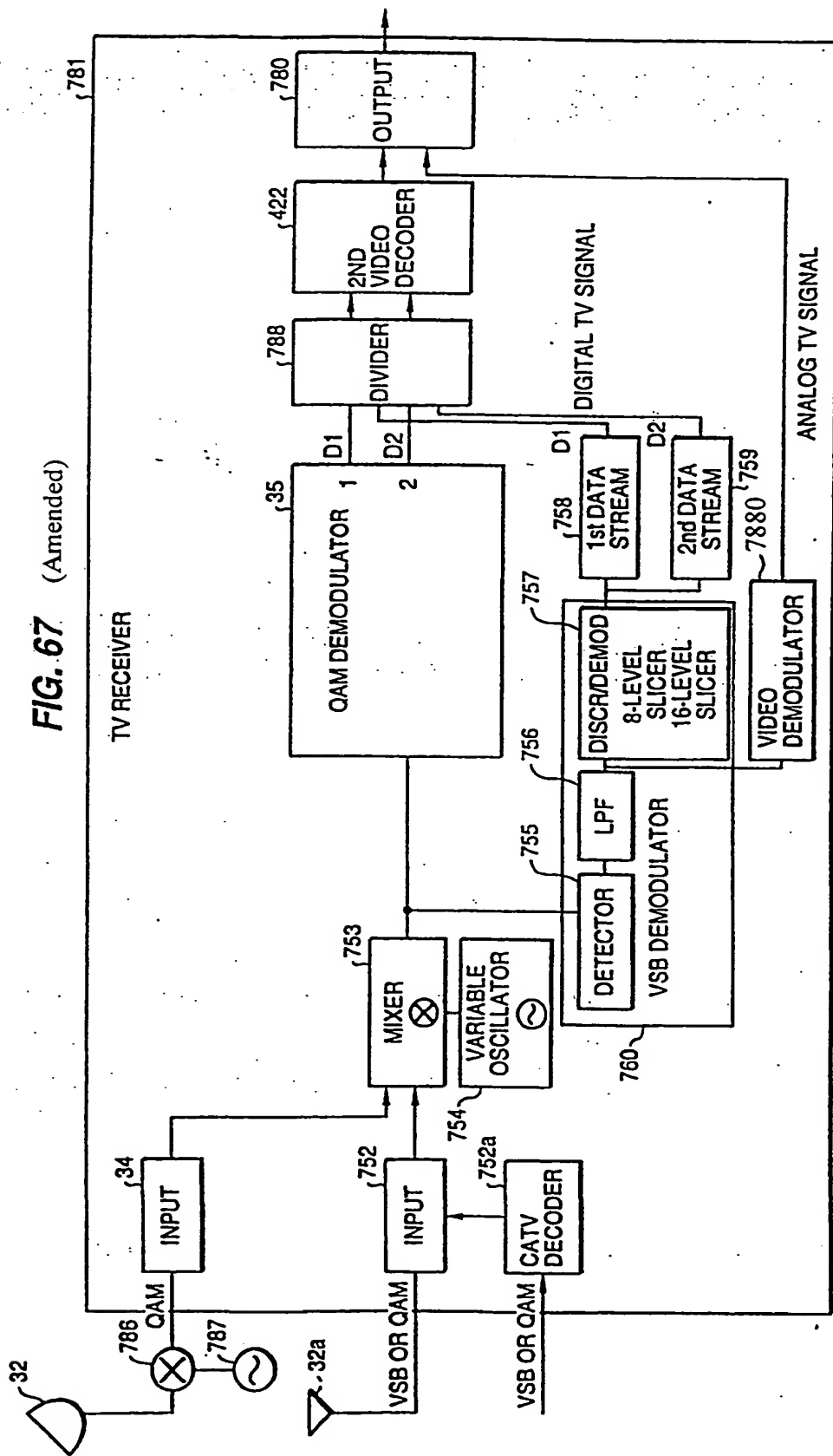


FIG. 67 (Amended)

3

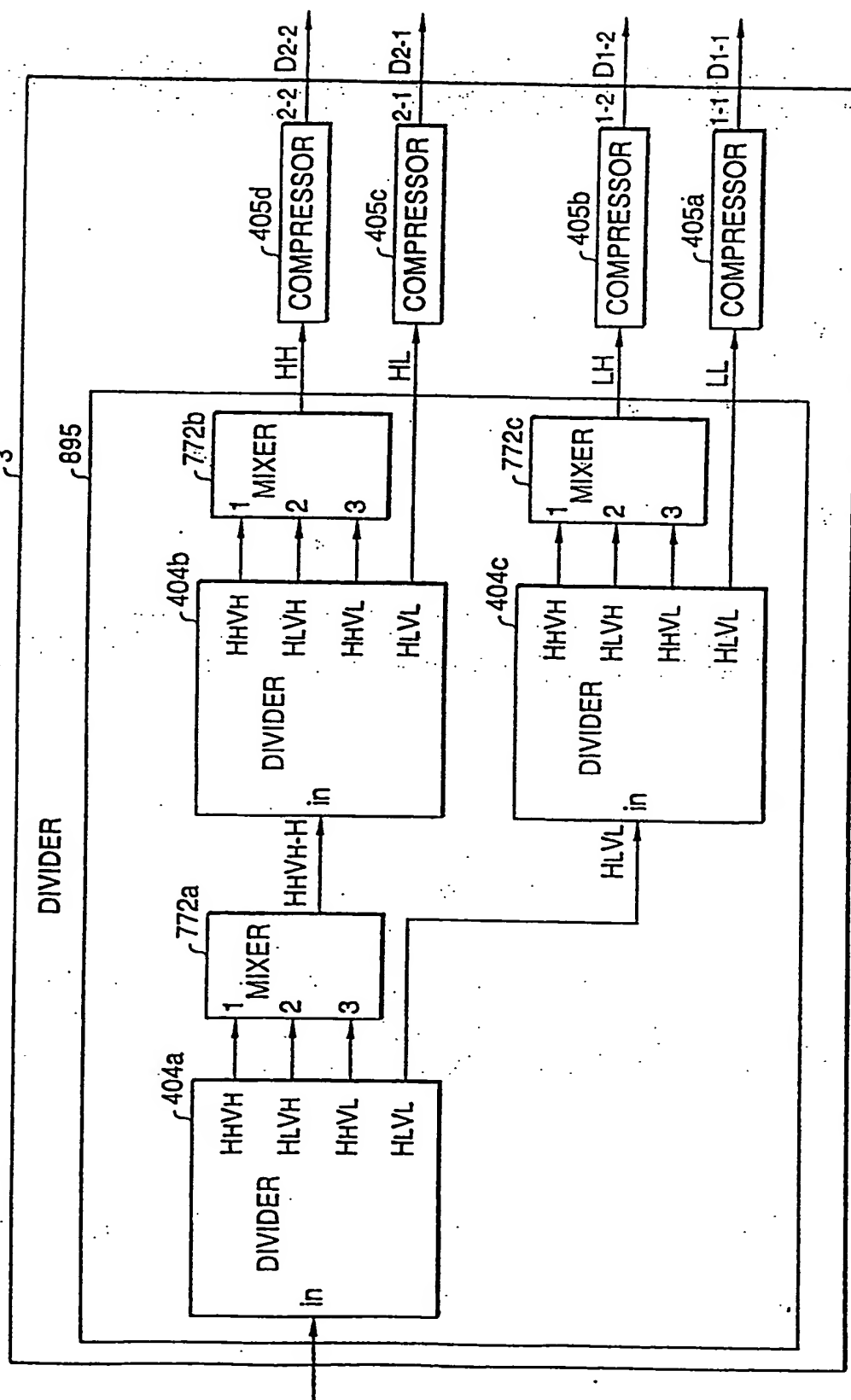
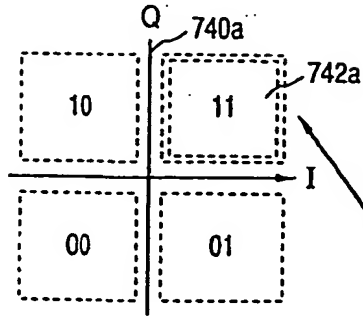
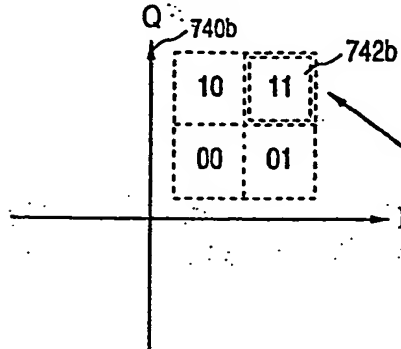


FIG. 112 (Amended)

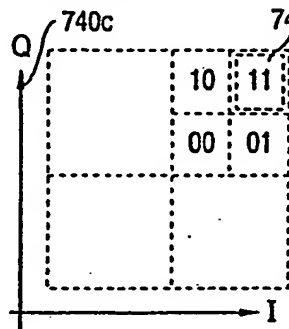
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



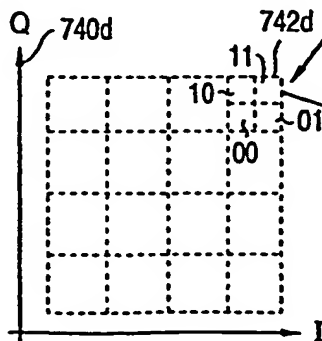
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)



SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)

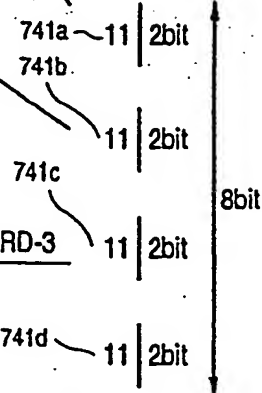


CODE WORD-1

CODE WORD-2

CODE WORD-3

CODE WORD-4



SIGNAL POINT
CODE WORD
11 11 11 11

FIG. 131 (Amended)

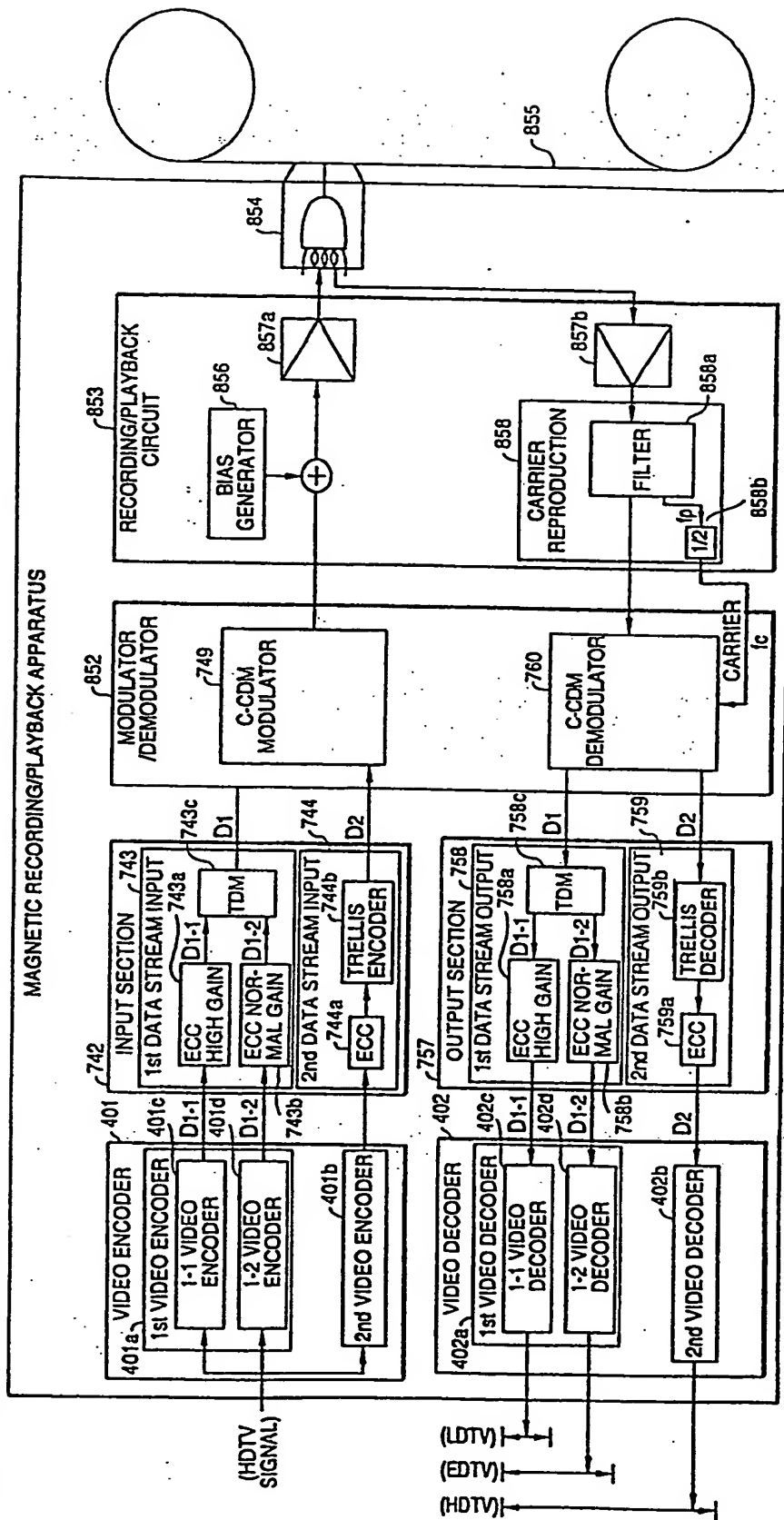


FIG. 138 (Amended)

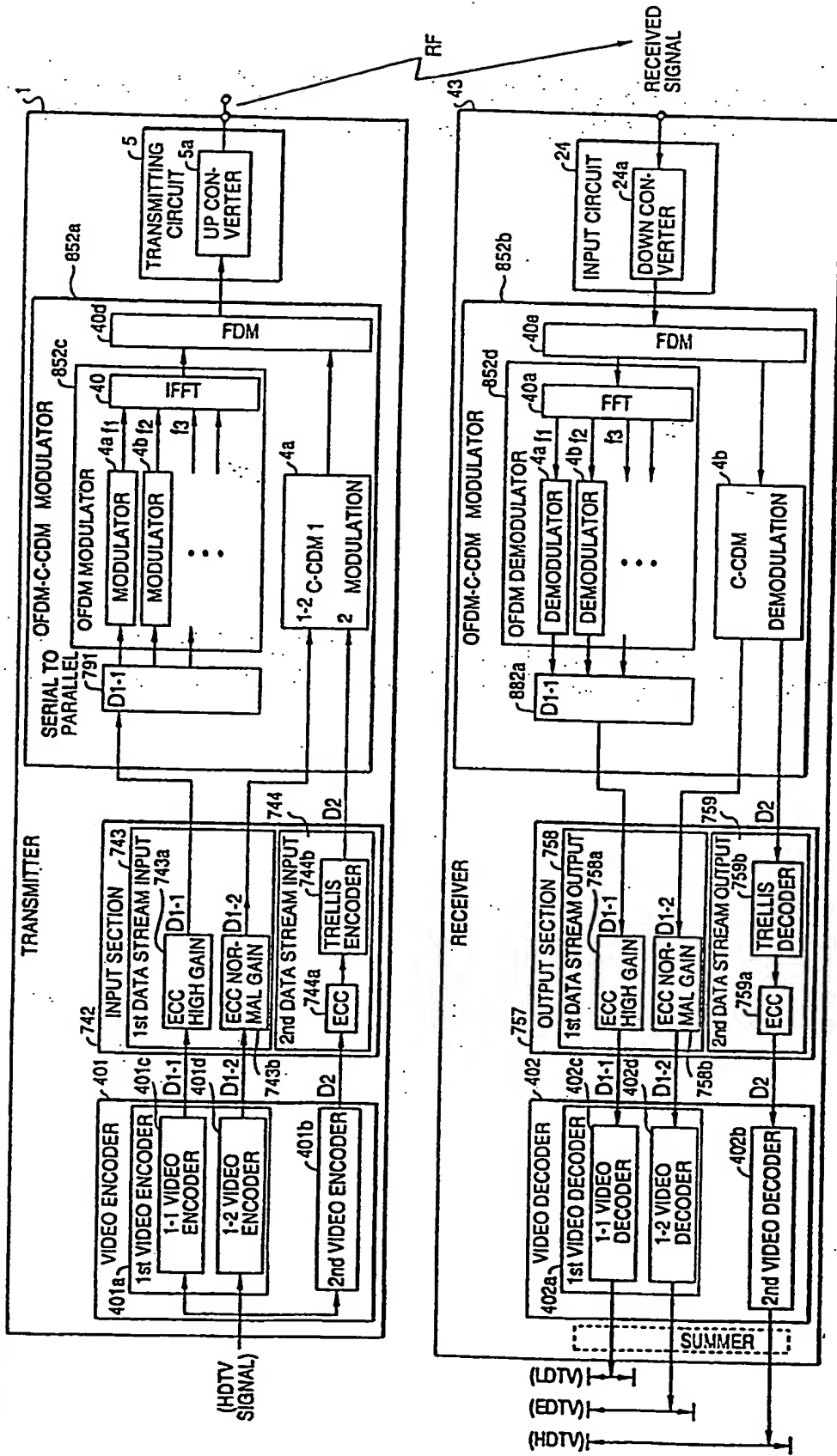


FIG. 144 (Amended)

The diagram illustrates a transmitter and receiver system. The **TRANSMITTER** section (left) processes an **(HDTV SIGNAL)** through a **VIDEO ENCODER 401** (containing 1-1 and 1-2 video encoders), an **INPUT SECTION 743** (with ECC, high gain, and TDM blocks), and a **TRELLIS ENCODER 744**. The output is a **SERIAL TO PARALLEL 791** stream, which is then processed by a **WEIGHTED OFDM-MODULATOR 4** (with subcarriers 4a f1 to 4f f8) and a **D/A CONVERTER 4e**. The final output is a **TRANSMIT CIRCUIT 5a** (UP CON-VERTER) emitting an **RF** signal.

The **RECEIVER** section (right) receives a **RECEIVED SIGNAL** through an **INPUT CIRCUIT 24a** (DOWN CON-VERTER) and an **A/D CONVERTER 40c**. The signal is then processed by a **WEIGHTED OFDM-DEMODULATOR 45** (with subcarriers 45a f1 to 45f f8) and a **SERIAL TO PARALLEL 852b** block. The output is a **PARALLEL TO SERIAL 852a** stream, which is then processed by an **OUTPUT SECTION 758** (with ECC, high gain, and TDM blocks) and a **TRELLIS DECODER 759**. The final output is a **SUMMER** block that combines the decoded signal with **(LDTV)** and **(EDTV)** signals to produce the **(HDTV)** output.

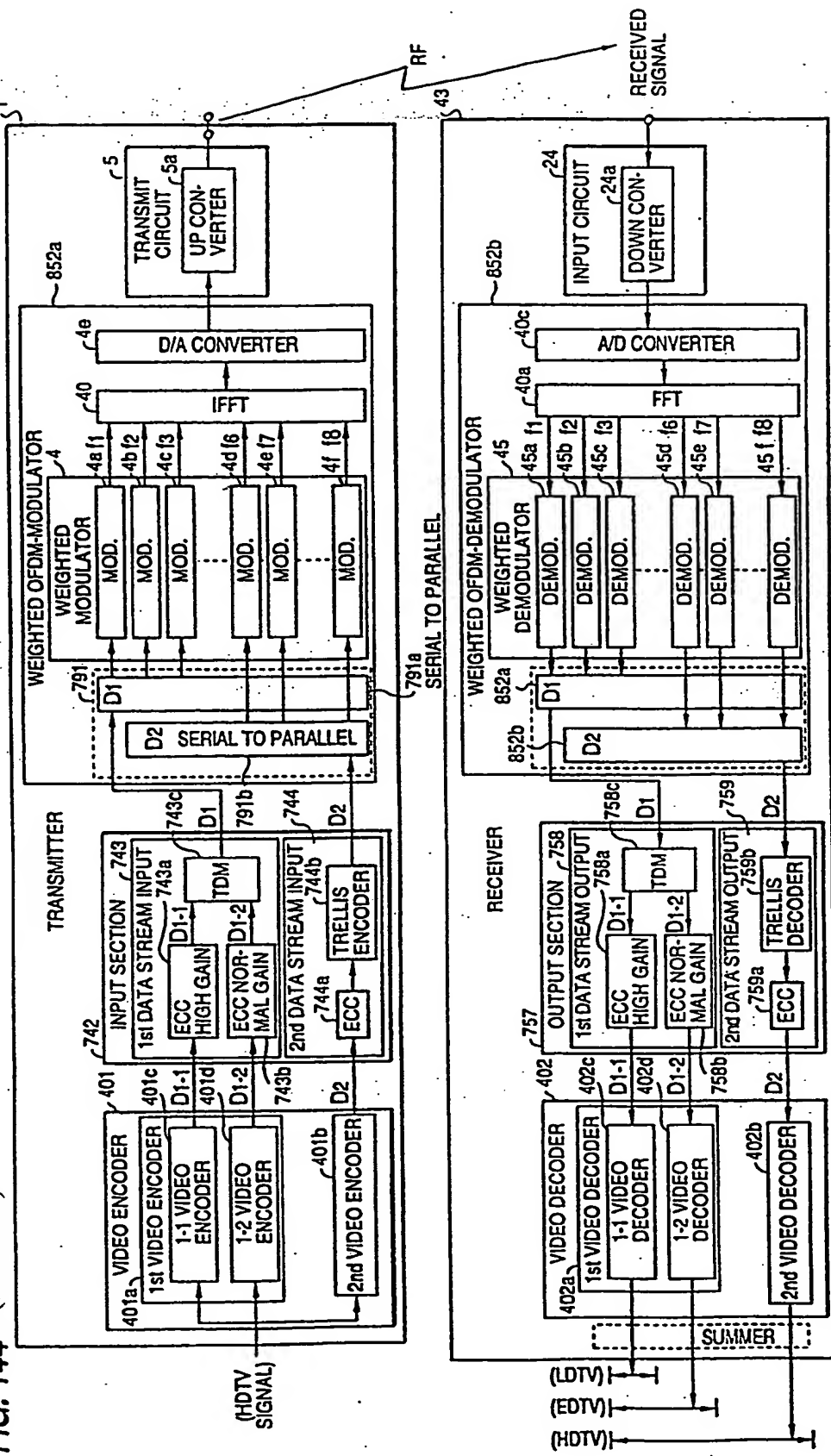


FIG. 169 (Amended)

